## Amendments to the Claims

This listing of claims will replace all prior listings of claims in the application.

## Listing of Claims

Claims 1-18 (Cancelled).

19. (New) A TFT display controller comprising:

a frame buffer operational to store TFT display data supplied from outside;

a timing controller;

a pixel pipe line (PPL) operational in response to signals generated by the timing controller to fetch and convert the TFT display data to a desired TFT display format; and

TFT display source/gate driver controls operational in response to signals generated by the timing controller to control representation of the TFT display data,

wherein all of the frame buffer, timing controller, pixel pipe line and TFT display source/gate driver controls are incorporated onto a single die, and

wherein the PPL outputs fixed data independent from the TFT display data to the source/gate driver controls in response to signals generated by the timing controller.

20. (New) The TFT display controller according to claim 19 wherein the timing controller switches the output of the TFT display data of the converted format from the PPL and the output of the fixed data in a constant cycle and a constant ratio of time.

21. (New) The TFT display controller according to claim 20 wherein black is displayed based on the fixed data.

22. (New) The TFT display controller according to claim 20 further comprising a means for determining a frequency for representation of the converted TFT display data on the TFT display, wherein the means for determining a frequency includes a programmable phase lock loop.

23. (New) A TFT display controller comprising:

a frame buffer operational to store TFT display data supplied from outside;

a timing controller;

a pixel pipe line (PPL) operational in response to signals generated by the timing controller to fetch and convert the TFT display data to a desired TFT display format; and

TFT display source/gate driver controls operational in response to signals generated by the timing controller to control representation of the TFT display,

wherein all of the frame buffer, timing controller, pixel pipe line and TFT display source/gate driver controls are incorporated onto a single die, and

wherein the PPL can be switched by the timing controller between a mode for FSC-TFT display and a mode for non-FSC-TFT display.

24. (New) The TFT display controller according to claim 20 wherein the constant period and the constant ratio of time are programmable.

25. (New) The TFT display controller according to claim 23 wherein the mode for FSC-TFT display is a display format including at least one color field for each of three colors in each frame, and wherein the mode for non-FSC-TFT display is a display format in which each frame is composed of one color field.

26. (New) The TFT display controller according to claim 25 wherein the TFT display controller has a plurality of power management modes, and wherein the mode for FSC-TFT display and the mode for non-FSC-TFT display are switched by the power management modes.

27. (New) The TFT display controller according to claim 20 further comprising a power management control (PMC) register for a plurality of power management modes, wherein the output of the TFT display data and the output of the fixed data are switched cyclically with a constant cycle and a constant ratio of time that are independent for each power management mode.

28. (New) A TFT display controller comprising:

a programmable timing controller;

a programmable pixel pipe line (PPL) operational in response to signals generated by the programmable timing controller to fetch and convert the TFT display data to a desired TFT display format;

a programmable color light sequencer operational in response to signals generated by the programmable timing controller to control a TFT display back light; and

programmable TFT display source/gate driver controls operational in response to signals generated by the programmable timing controller to control representation of the TFT display data converted by the PPL on a desired TFT display selected from the group consisting of a field sequential color TFT display and a non-field sequential color TFT display.

29. (New) The TFT display controller according to claim 28 wherein the frame buffer, PPL, color light sequencer,

programmable source/gate driver controls and programmable timing controller are integrated onto a single die.

30. (New) The TFT display controller according to claim 28 further comprising a programmable phase lock loop responsive to data stored therein to determine a frequency for representation of the TFT display data converted by the PPL.

31. (New) The TFT display controller according to claim 28 wherein the PPL comprises a plurality of parallel pixel pipes.

32. (New) The TFT display controller according to claim 31 wherein the PPL further comprises white and black fixed color data registers.

33. (New) The TFT display controller according to claim 32 wherein the PPL further comprises path select logic having a display raster setting (DRS) register, wherein data stored in the DRS register determines the desired TFT display format.

34. (New) The TFT display controller according to claim 28 further comprising a power management control (PMC) register, wherein data stored in the PMC register determines an output frequency associated with a PLL such that the PLL controls PPL data paths to manage power consumption of the PPL.

35. (New) The TFT display controller according to claim 28 wherein the programmable timing controller comprises field controls and sub-field controls operational to generate field and sub-field timing signals for the PPL and the back light.

36. (New) The TFT display controller according to claim 28 wherein the representation of the field sequential color

TFT display includes at least one color field for each of three colors in each frame, and wherein the representation of the non-field sequential color TFT display includes frames each consisting of one color field.

37. (New) The TFT display controller according to claim 36 wherein the TFT display controller has a plurality of power management modes, and wherein the representation of the field sequential color TFT display and the representation of the non-field sequential color TFT display are switched by the power management modes.

38. (New) A TFT display controller comprising:

means for storing TFT display data;

means for storing power management control data;

means for generating timing control signals;

means for fetching and converting the TFT display data to a desired TFT display format in response to the timing control signals;

means for controlling a TFT display backlight in response to the timing control signals;

means responsive to the timing control signals to control representation of the converted TFT display data on a desired TFT display selected from the group consisting of a field sequential color TFT display and a non-field sequential color TFT display; and

means for determining a frequency for representation of the converted TFT display data in response to data stored in the means for storing power management control data,

wherein the means for storing TFT data, means for generating timing control signals and means for fetching and converting the TFT display data to a desired TFT format are integrated onto a single die.

39. (New) The TFT display controller according to claim 38 wherein the means for fetching and converting the TFT display data to a desired TFT display format comprises a programmable pixel pipe line which includes white and black fixed color data registers.

40. (New) The TFT display controller according to claim 38 wherein the means for determining a frequency for representation of the converted TFT display data on the TFT display comprises a programmable phase lock loop.

41. (New) The TFT display controller according to claim 38 wherein the representation of the field sequential color TFT display includes at least one color field for each of three colors in each frame, and wherein the representation of the non-field sequential color TFT display includes frames each consisting of one color field.

42. (New) The TFT display controller according to claim 41 wherein the representation of the field sequential color TFT display and the representation of the non-field sequential color TFT display are switched in response to the data stored by the means for storing power management control data.